

FIG.1
CONVENTIONAL ART

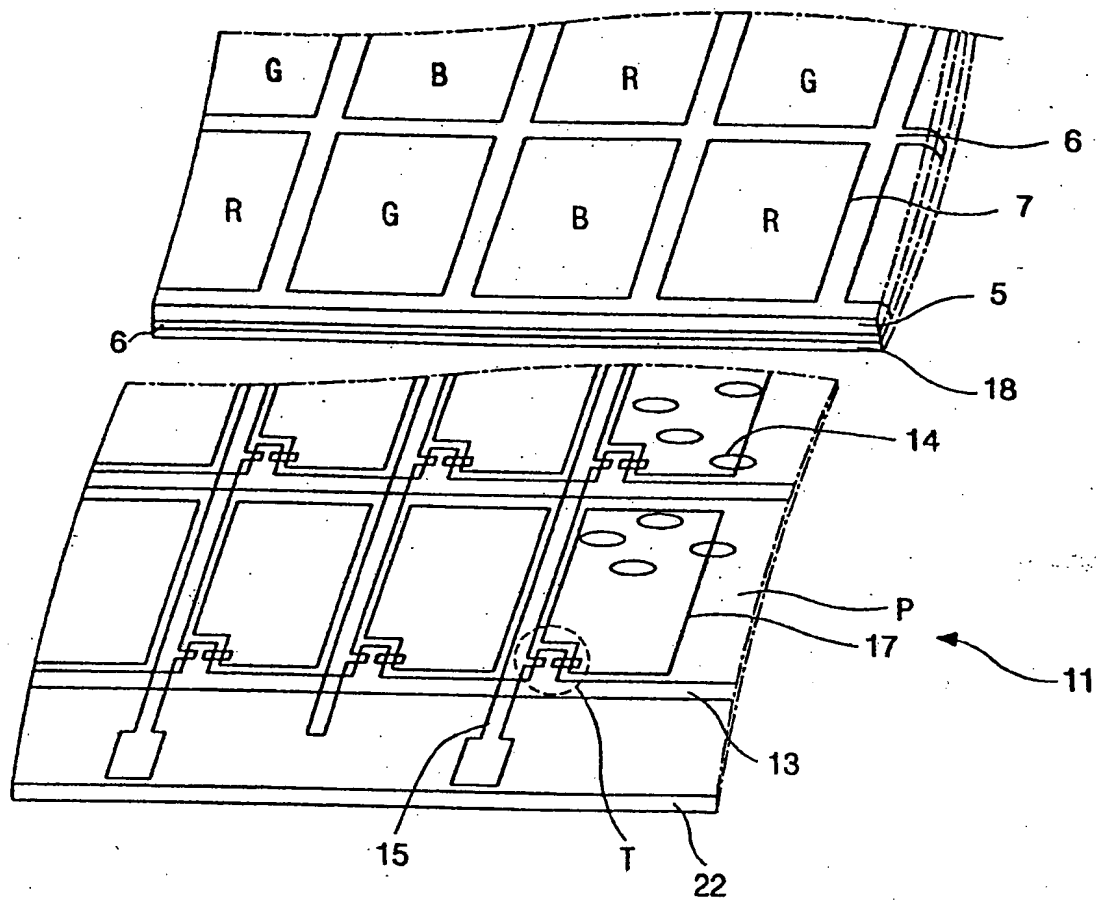
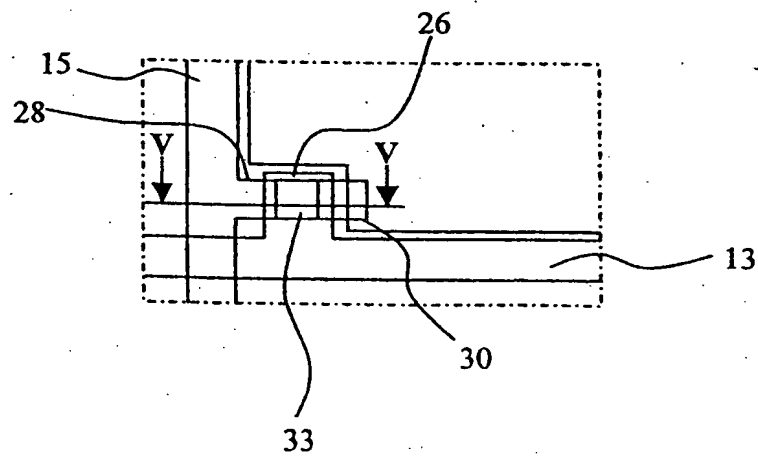
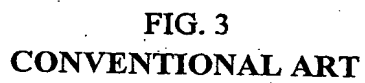


FIG. 2
CONVENTIONAL ART



REPLACEMENT SHEET

FIG. 4A
CONVENTIONAL ART

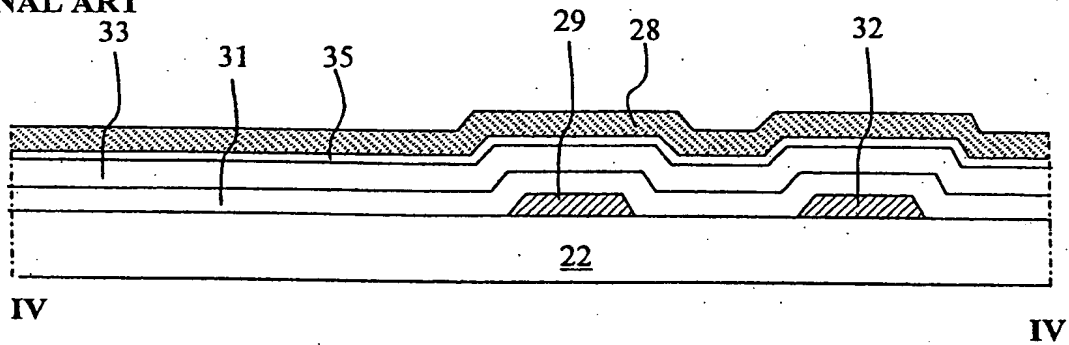


FIG. 4B
CONVENTIONAL ART

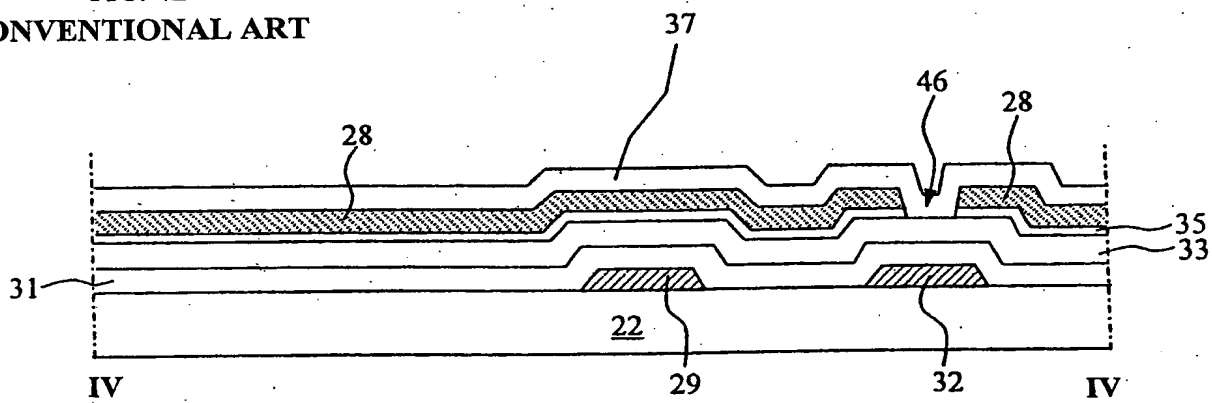
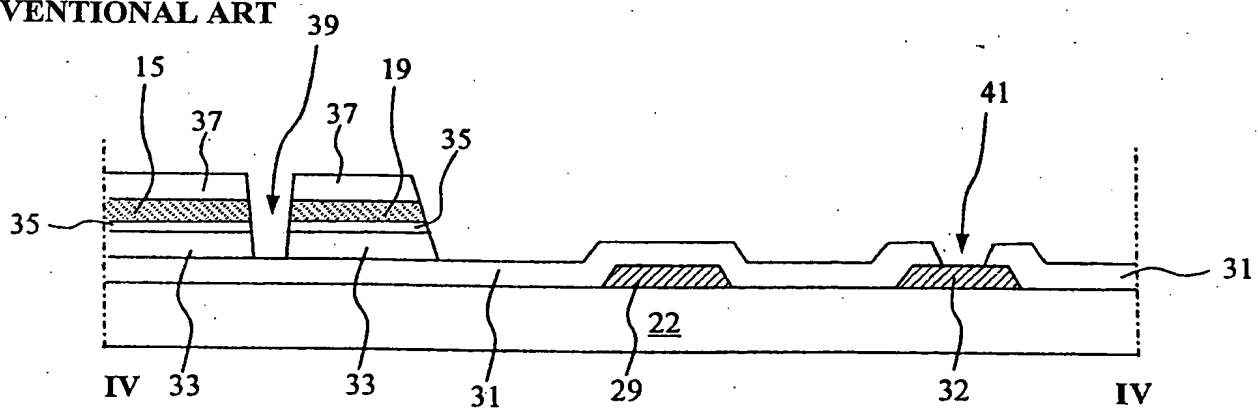


FIG. 4C
CONVENTIONAL ART



REPLACEMENT SHEET

FIG. 4D
CONVENTIONAL ART

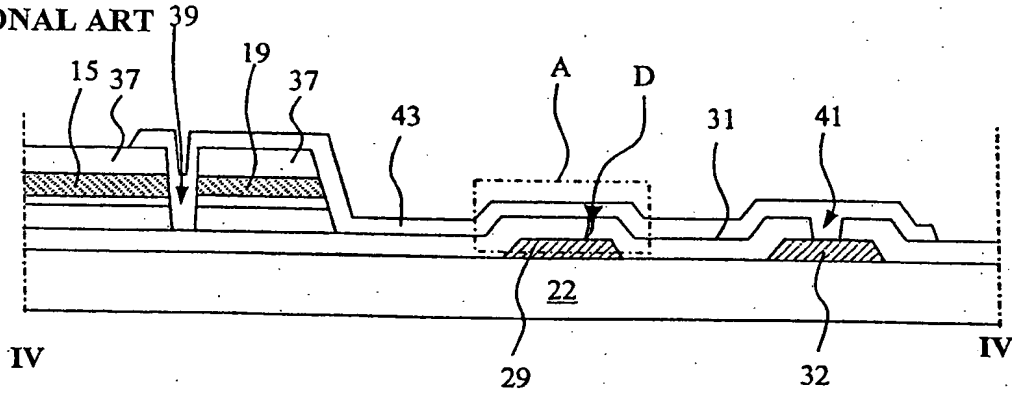


FIG. 5A
CONVENTIONAL ART

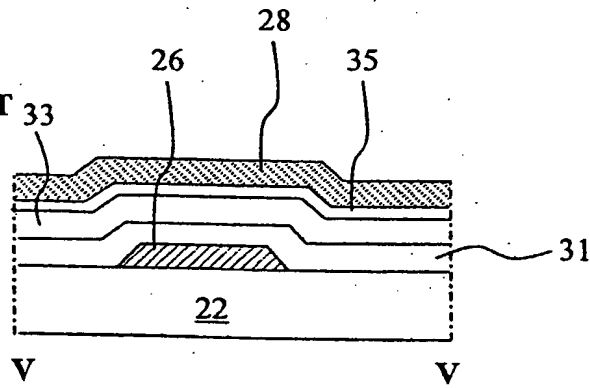
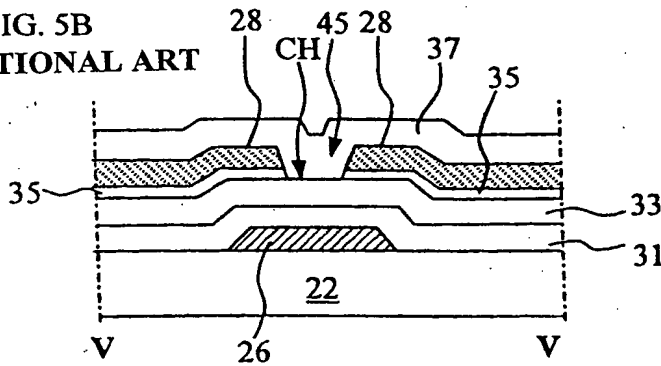


FIG. 5B
CONVENTIONAL ART



REPLACEMENT
SHEET

FIG. 5C
CONVENTIONAL ART

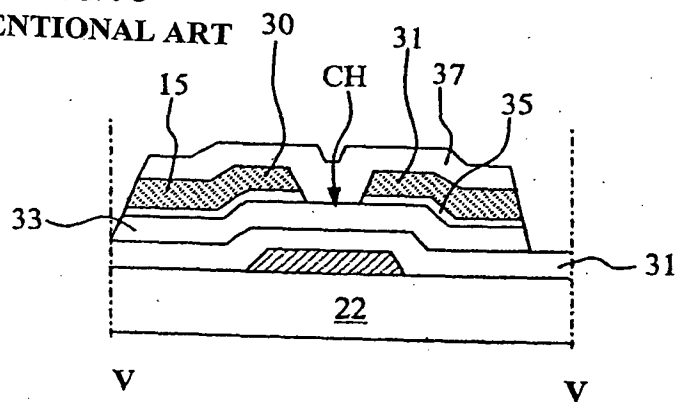


FIG. 5D
CONVENTIONAL ART

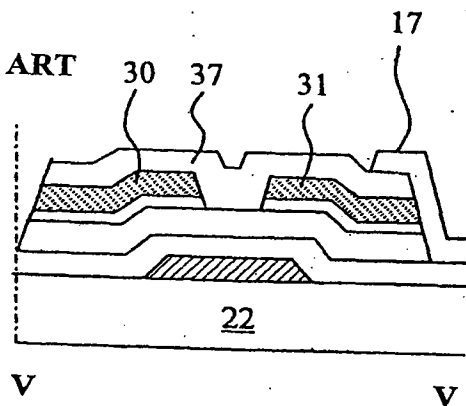


FIG. 6

FIG. 6 is a cross-sectional view of a semiconductor device. The device features a grid of conductive lines. The top section shows a grid of lines with labels 140, 141, 151, 132, 129, 142, 143, 139, 119, and VIII. A dashed line separates this from the bottom section, which shows a more complex structure with labels 118, 117, 113, 115, C, P, and T. A vertical dashed line is on the left, and a horizontal dashed line is in the middle.

This diagram is a cross-sectional view of a semiconductor device. It shows a substrate with a gate structure on top. The gate structure includes a gate dielectric layer (115) and a gate electrode (126). A channel region (130) is defined by the gate structure. A source/drain region (133) is located on the side of the channel region. A contact layer (128) is shown on the side of the channel region. Two arrows labeled 'IX' point to the channel region (130) and the contact layer (128).

... ..)

FIG. 8A

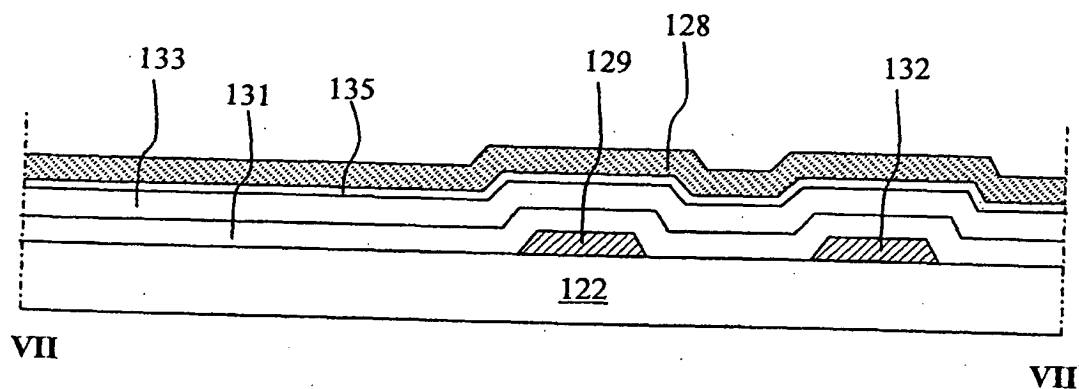


FIG. 8B

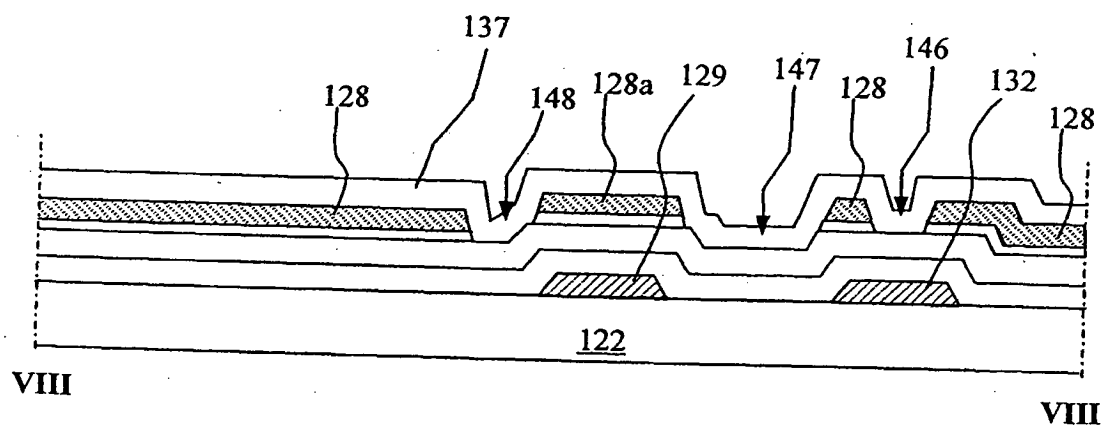
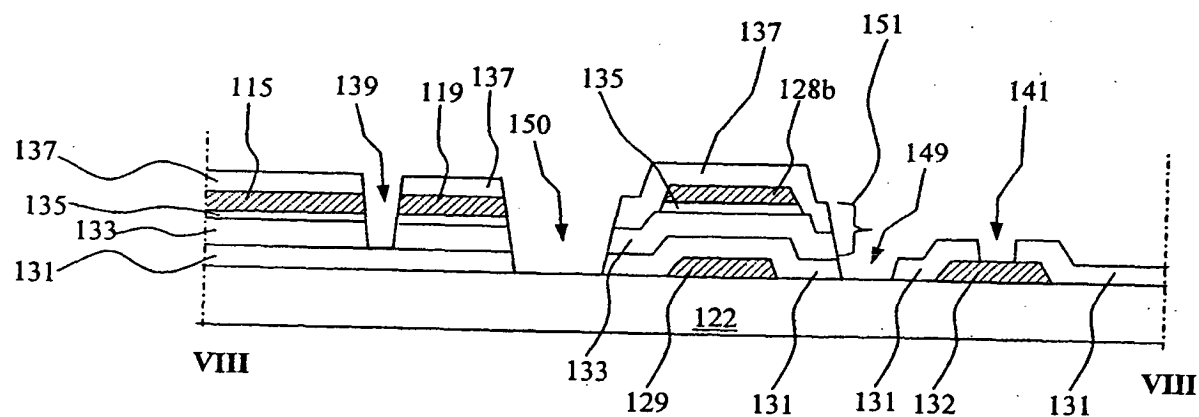


FIG. 8C



REPLACEMENT SHEET

FIG. 8D

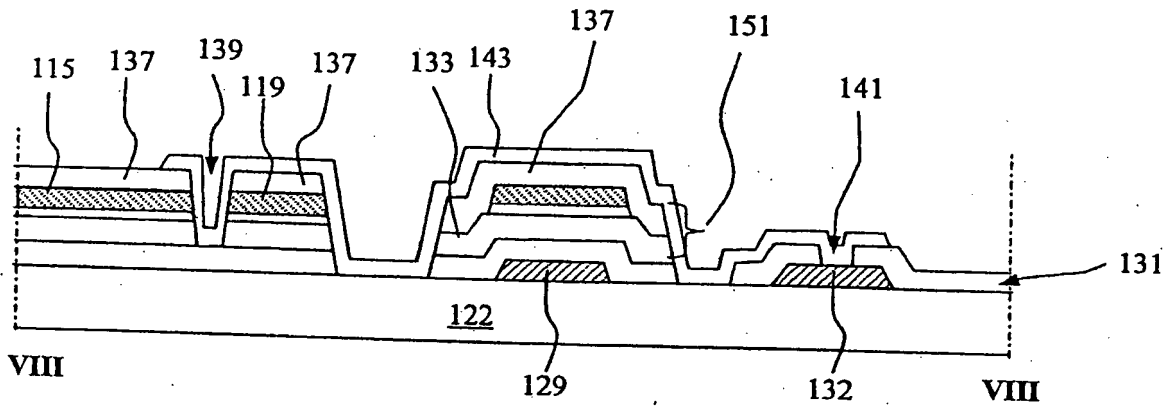


FIG. 9A

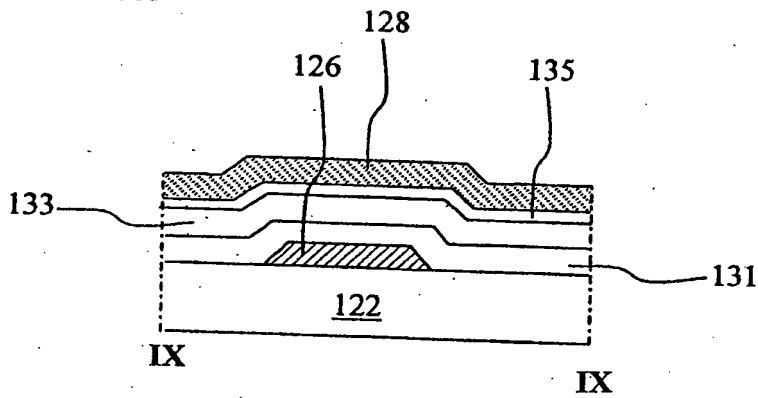
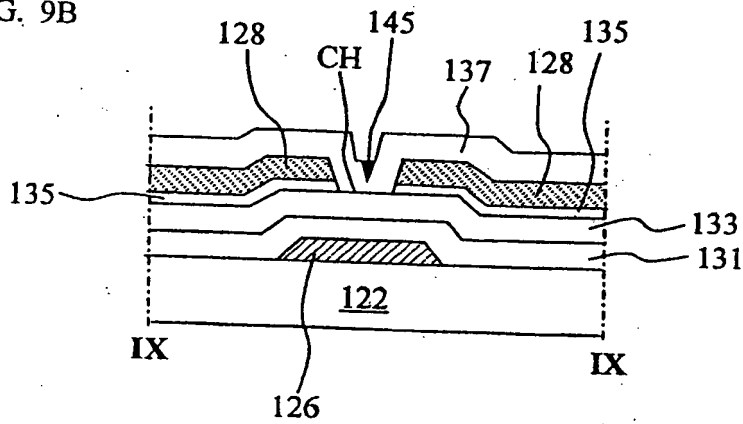


FIG. 9B



REPLACEMENT
SHEET

